WHAT IS CLAIMED IS:

- 1 1. A method for minimizing the number of appearances of a given state in a code word
- 2 generated from a data word comprising:
- 3 counting the number of times the given state appears in the data word;
- 4 if the count is greater than half of a total number of bits in the data word, then
- 5 inverting the data word;
- 6 setting a weight bit to the given state; and
- 7 else
- 8 setting the weight bit to an inverse of the given state.
- 1 2. The method of claim 1, wherein the code word comprises the weight bit combined with
- 2 the inverted data word if the count is greater than half the total number of bits in the data word,
- 3 else the code word comprises the weight bit combined with the data word.
- 1 3. The method of claim 2, wherein the weight bit is a single bit in length.
- 1 4. The method of claim 1, wherein the given state is a zero state, and the weight bit is set to
- 2 zero if the number of zeros in the data word is greater than half the total number of bits in the
- data word, else the weight bit is set to one.
- 1 5. The method of claim 1, wherein the given state is a one state, and the weight bit is set to
- 2 one if the number of ones in the data word is greater than half the total number of bits in the data
- word, else the weight bit is set to zero.

- 1 6. The method of claim 1, wherein the method can be used to generate code words for use in
- 2 a transmission system with an asymmetrically terminated transmission line, and wherein the
- 3 given state is complementary to the termination of the transmission line.

- 1 7. A circuit comprising:
- 2 an encoder coupled to a data input, the encoder containing circuitry to convert data words
- 3 from the data input into code words with a minimized number of occurrences of a given state;
- 4 and
- 5 a transmitter coupled to the encoder, the transmitter containing circuitry to inject the code
- 6 words onto a transmission line, wherein the transmission line is asymmetrically terminated.
- 1 8. The circuit of claim 7, wherein the code word is one bit longer than the data word.
- 1 9. The circuit of claim 7, wherein the encoder comprises:
- 2 a weight calculator coupled to the data input, the weight calculator containing circuitry to
- determine a count of the number of times the given state appears in a data word and to compute a
- 4 weight bit based on the count; and
- 5 a plurality of logic blocks coupled to the data input and the weight calculator, wherein
- 6 each logic block is coupled to a single bit of the data input and the weight bit computed by the
- 7 weight calculator, the logic block to combine the inputs to produce a bit of the code word.
- 1 10. The circuit of claim 9, wherein the logic block is implemented as an exclusive-nor
- 2 (XNOR) logic gate.
- 1 11. The circuit of claim 9, wherein there is one logic block for each bit in the data word.
- 1 12. The circuit of claim 9, wherein the weight calculator comprises:
- a first hierarchy of M switches, wherein M is less than the number of bits in the data
- word, wherein each switch is controlled by a bit of the data word, a switch to route an input to an
- 4 output depending on the value of the bit controlling it;

- 5 a second hierarchy of switches, wherein for each switch in the first hierarchy of switches,
- 6 there is a pair of switches in the second hierarchy of switches, wherein each pair of switches is
- 7 controlled by a bit of the data word; and
- 8 a logic block coupled to the second hierarchy of switches, the logic block containing
- 9 circuitry to compute the weight bit.
- 1 13. The circuit of claim 12, wherein one half of the data bits in the data word is coupled to
- 2 the switches in the first hierarchy of switches and the remaining data bits in the data word are
- 3 coupled to the pairs of switches in the second hierarchy of switches.
- 1 14. The circuit of claim 13, wherein if a data bit is used to control a switch in the first
- 2 hierarchy of switches, then the data bit is not used to control a pair of switches in the second
- 3 hierarchy of switches.
- 1 15. The circuit of claim 12, wherein an input to the switches in the first hierarchy of switches
- 2 is a low voltage potential.
- 1 16. The circuit of claim 12, wherein each switch is a one input to two output switch, and
- 2 wherein the inputs to a pair of switches in the second hierarchy of switches are the two outputs of
- a switch from the first hierarchy of switches.
- 1 17. The circuit of claim 12, wherein a switch can be implemented as a one-input to two-
- 2 output multiplexer.
- 1 18. The circuit of claim 7, wherein the transmission line is pulled to a voltage potential.

- 1 19. The circuit of claim 18, wherein the transmission line is pulled to a high voltage potential
- 2 and the given state is a low voltage potential.
- 1 20. The circuit of claim 18, wherein the transmission line is pulled to a low voltage potential
- 2 and the given state is a high voltage potential.

- 1 21. A transmission system comprising:
- an encoder coupled to a data input, the encoder containing circuitry to convert data words
- 3 from the data input into code words with a minimized number of occurrences of a given state;
- 4 a transmitter coupled to the encoder, the transmitter containing circuitry to inject the code
- 5 words onto a transmission line, wherein the transmission line is asymmetrically terminated;
- a receiver coupled to the transmission line, the receiver containing circuitry to receive
- 7 code words from the transmission line; and
- 8 a decoder coupled to the receiver, the decoder containing circuitry to convert code words
- 9 into data words.
- 1 22. The transmission system of claim 21, wherein each code word comprises a code block
- 2 and a weight bit, and wherein the decoder comprises a plurality of logic blocks coupled to the
- 3 receiver, wherein each logic block is coupled to a single bit of the code block and the weight bit,
- 4 the logic block to combine the inputs to produce a bit of the data word.
- 1 23. The transmission system of claim 22, wherein the logic block can be implemented as an
- 2 exclusive-nor (XNOR) logic gate.